Remarks/Arguments

Reconsideration of this application is requested.

Claim Status

Claims 1, 2, 4-9 and 11-14 are pending. Claims 4-7, 11 and 12 are amended.

Specification Objections

The Action objects to the disclosure and asserts that "second block" on page 3 of the specification, lines 3 and 5, should be "first block" based on the preceding description of the first and second blocks on page 2 of the specification. Applicant respectfully traverses this objection and submits that the Examiner has misunderstood applicant's disclosure (and claims).

Attached to this amendment is a copy of applicant's Fig. 1, with emphasis added to the "first block" and "second block" of circuits. Tracking paragraph [0006] of page 2, the image forming apparatus includes a plurality of processing circuits categorized into first and second blocks with respect to respective functions of the circuits. Power transformer T has a plurality of secondary windings T2A and T2B. First power supply unit A ("continuous power block") *always feeds DC current to the first block of processing circuits* from at least one of the secondary windings T2A. Thus, as seen in FIG. 1, the first block of processing circuits comprises the CPU and modem, which are always fed DC current from first power supply unit A via line La. A second power supply unit B ("power save block") feeds DC power to the second block of processing circuits from the secondary windings (T2B) other than the above-mentioned at least one of the secondary windings. Thus, the second block of processing circuits includes the image processor, printer, scanner, communication unit and operational amplifiers of filters and amplifier circuits.

At least one switch SW interrupts DC current between the secondary windings T2B and the second block of processing circuits. A control unit controls switches SW such that DC current from secondary windings T2B to the second block of processing circuits is interrupted in a power save mode, and such that DC

current is fed to the secondary block of processing circuits from the secondary windings T2B in a normal mode.

Continuing on to paragraph [0007], the control unit (CPU) may be operated with DC current from the first power supply A (via signal processor power source line La). The image forming apparatus may further include a voltage converting circuit (DC/DC converters 6, 6' and terminal regulator 7) for converting DC voltage (e.g. +5V) of the first power supply unit A to DC voltage of another level (e.g. +12V, -12V and +3.3V) such that the DC voltage of another level *is fed to the second block of processing circuits* (page 3, line 3). As is clearly seen in FIG. 1, the DC voltages of another level (e.g. +12V, -12V and +3.3V) come from the converting circuit (DC/DC converters 6, 6' and terminal regulator 7) to the image processor, printer, scanner, communication unit and operational amplifiers of filter and amplifier circuits which, as described above, comprise the second block of processing circuits.

Lines 3-5 of page 3 go on to correctly state, as described above, that the second block of processing circuits may include an image processing circuit, a printing unit, an image scanning unit and a communication control unit, and that the DC current may be fed to the second block of processing circuits from the voltage converting circuit in the power save mode. Thus, the descriptions of the first and second blocks of processing circuits are correct throughout the description on pages 2-3. The supply of power from the voltage converting circuit to the second block of processing circuits is a critical feature of the present invention since, if switches SW are opened, the supply of power to the second block of processing circuits from power save block B is cut off.

Claim Objections

The Action also objects to claim 1 and asserts that "second block" in the last line of claim 1 should be "first block". For the same reasons as discussed with respect to the specification, above, applicant respectfully traverses this objection. The last line of claim 1 correctly states that the DC voltage of another level (i.e. the voltage output from terminal regulator 7 and DC/DC converters 6, 6') is fed to the

second block of processing circuits (image processor, printer, scanner, communication unit, operational amplifiers of filter and amplifier circuits) in the power save mode (i.e. when switches SW are open so that power is not supplied to the second block of circuits by power save block B).

Claims 4-7 are objected to as depending from canceled claim 3, and claims 11 and 12 are objected to as depending from canceled claim 10. In response, claims 4-7 are amended to depend from claim 1 and claims 11 and 12 are amended to depend from claim 9.

Claim Rejections – 35 USC 103(a)

Claims 1, 2, 4-9 and 11-14 are rejected under 35 USC 103(a) as obvious over Iwasaki (US 6,097,616) in view of Takeda (US 5,760,494). For the reasons set forth below, applicant respectfully traverses the rejections.

The Action states that "Iwasaki fails to disclose a voltage converting circuit for converting DC voltage of the first power supply to DC voltage of another level such that DC voltage of another level is fed *to the first block of processing circuits* in the power save mode". This statement reflects and continues the misunderstanding discussed above, since applicant's claims require that the voltage converting circuit convert DC voltage of the first power supply (which is fed to the first block of processing circuits) to DC voltage of another level which is fed to *a second block of processing circuits*, and not the first block.

The Action cites DC/DC converter 5 of Takeda as supplying the teachings missing from Iwasaki. Applicant respectfully disagrees. Takeda's DC/DC converter 5 does not interact with first and second blocks of processing circuits as is required by applicant's claims. DC/DC converter 5 is controlled by microcomputer 50 (col. 3, lines 42-43.) and converts high voltage DC power from a smoothing circuit 4 to stabilized low-voltage DC power sent to a control panel 6 and a drive system 7. Microcomputer 50 cannot correspond to the "first block" of processing circuits of applicant's claims, since DC/DC converter does not convert a DC voltage supplied to microcomputer 50 to a DC voltage of another level that is fed to a second block of

processing circuits. Moreover, control panel 6 and drive system 7 cannot be considered a second block of circuits as recited in claims 1 and 8, since they are not subject to interruption in supply of power from another source in a power save mode. Applicant also notes that a regulator 15 supplies electric power to microcomputer 50 (column 3, lines 38-41), however, regulator 15 does not convert power supplied to a first block of circuits into power supplied to a second block of circuits in a power save mode, as is required by claims 1 and 8.

Thus, Iwasaki and Takeda, taken alone or in combination, lack disclosure of a voltage converting circuit that converts DC voltage of a first power supply (which is fed to the first block of processing circuits) to DC voltage of another level which is fed to a second block of processing circuits in a power save mode where the second block of processing circuits is cut off from a second power supply. Since Iwasaki and Takeda do not disclose or suggest each and every element of claims 1 and 8, it cannot render those claims, or claims depending therefrom, obvious. For these reasons, the rejections of claims 1, 2, 4-9 and 11-14 as obvious over Iwasaki and Takeda should be withdrawn.

Conclusion

This application is in condition for allowance. The Examiner is urged to telephone the undersigned to discuss any issues in connection with this response. Any fees due with this response may be charged to our Deposit Account No. 50-1314.

Respectfully submitted,
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